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NEW DSP-BASED FIRING GENERATOR FOR THE PPPL AC/DC CONVERTERS

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***Abstract*— The control systems of the National Spherical Tokamak Experiment (NSTX) are undergoing a significant upgrade. The new digital firing generator (FG) is a key component. The new FG is designed and implemented using two Texas Instrument (TI) digital signal processors (DSP) which accept the firing angle, convert and bypass command from the real time computer using the Front Panel Data Port (FPDP) protocol. It generates the six firing pulses to the thyristor power supplies for the NSTX magnet coils that operate with a variable frequency AC source. This paper provides a detailed description of the FG system, the optical communication link, the phase lock loop circuit and the DSP hardware and software. Some test results using the new FG for the power supply are also included.**

Keywords—firing generator; thyristor; phase locked loop; digital signal processor

I. INTRODUCTION

A new firing generator (FG) has been designed and implemented for the Transrex 12-pulse thyristor AC/DC converters that were originally deployed at the Princeton Plasma Physics Laboratory (PPPL) for the Tokamak Fusion Test Reactor (TFTR) and are now in use for the NSTX. These power supplies are powered by a three winding transformer with a rating of l3.8kV/750V. The transformer has a polygon primary and Δ/Y secondary windings. The polygon is arranged to produce +7.5º or -7.5º phase shift [1]. Each power supply has two sections, A and B. Each section has a power module which has a rating of 1kV, 24kA- 6 seconds equivalent square wave (ESW), for every 300 seconds. Each section also has a bypass module designed to carry the full load current when the power module thyristors are suppressed and bypassed.

The new FG receives commands generated by the Power Supply Real Time Control (PSRTC) software algorithms through the optical communication link. The commands include the firing angle, the convert bit and the bypass bit. The new FG has two major operational requirements [2]. First, it must deliver 6 synchronized firing pulses to the individual 6-pulse thyristor bridges supplied by a variable-frequency AC voltage source between 50 Hz to 90 Hz. This frequency can ramp at a rate of up to 10 Hz/second. Second, it must prevent commutation failure during inversion by limiting the firing angle. The maximum allowable firing angle has to be calculated in real time as a function of the input voltage frequency, the load current, the transformer leakage inductance and the input voltage amplitude.

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The new FG is designed using two TI TMS320F28335 DSP. One is called the master DSP and the other is called the slave DSP. The master DSP is used to receive the command from the real time control computer. It also calculates the firing angle limit and sends the final firing angle to the slave DSP. The slave DSP generates the firing pulses using phase locked loop (PLL) technology which is immune to the transients and harmonic distortions in the supply voltage.

II. FIRING GENERATOR AND COMMUNICATION SYSTEM

The PSRTC software runs on a real time computer. It transmits commands through fiber optic links using the FPDP protocol. The new FPDP Output Module Serial (FOMS) are designed to receive the FPDP word from the PSRTC. Based on the address in the FPDP word, it passes the control command through another fiber optic link to the specific FOMS receiver inside the new FG. The FG accepts the firing angle and generates the 6 firing pulses to the thyristor bridges. Under fault conditions the fault detector sends a fault signal to the FG which then blocks the firing pulses to the thyristor bridges and sends the bypass command to the bypass thyristors. The system diagram for the optical communications link and the FG is shown in Fig. 1.

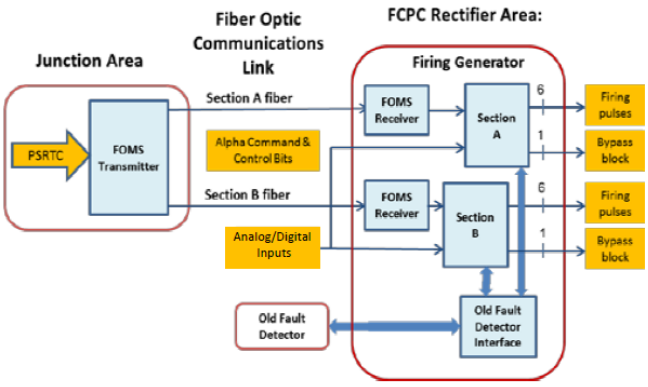

Fig. 1. System diagram for the communications link and the firing generator

The front panel of the FG is shown in Fig. 2. The top part is for section A and the bottom part is for section B. The six firing pulses can be monitored through the front panel BNC connectors. The LCD display shows the voltage, the current, the line frequency and the firing angle information. The keyboard is used to input the configuration data for the power supply.

Fig. 2. The front panel of the firing generator

A. Optical Communications Link

1) FOMS transmitter module

The FOMS transmitter module is a VME-format board that is used to receive 32-bit FPDP word from the PSRTC real time computer. It has two 1024-words FIFO to buffer the FPDP data. A Xilinx complex programmable logic device (CPLD) XC95288 is programmed to perform several key functions, such as the FIFO update, data routing, parity checking and broadcasting. The 16 bit data of the firing angle, the convert and the bypass bit are sent to the CPLD XC95144. It uses Manchester coding to send the data through the optical fiber to the FOMS receiver in the FG. Fig. 3 shows the FOMS transmitter function block diagram. Fig. 4 shows the real FOMS transmitter circuit board.

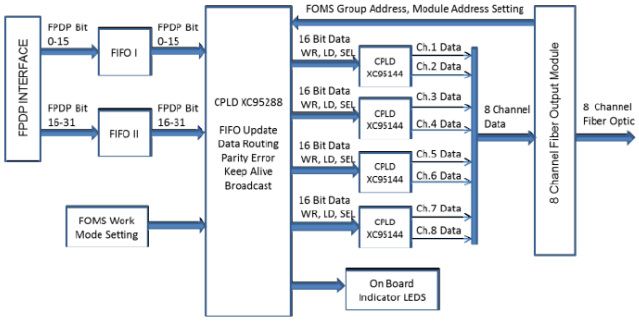

Fig. 3. FOMS transmitter function block diagram

Fig. 4. FOMS transmitter circuit board

2) FOMS receiver module

The FOMS receiver module inside the FG is designed to receive the 16 bit control word from the FOMS Transmitter through the fiber optic cable. It checks the parity error and passes the control command to the DSP control board in the FG. The FOMS receiver function block diagram is shown in Fig. 5. The FOMS receiver circuit board is shown in Fig. 6.

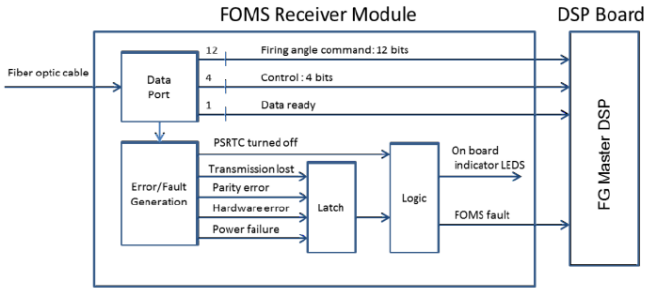

Fig. 5. FOMS receiver function block diagram

B. Firing Generator Hardware

The new FG has five circuit boards as shown in Fig. 6. Two separate FOMS receiver boards for the power supply section A and B. Two DSP control boards for section A and B. One phase lock loop board is used to generate the pulse train runs at 3600*f Hz. Here f is the three phase AC input frequency which varies from 50-90 Hz. The DSP accept the PLL pulse as the counter clock. The firing angle can be calculated based on the pulse count.

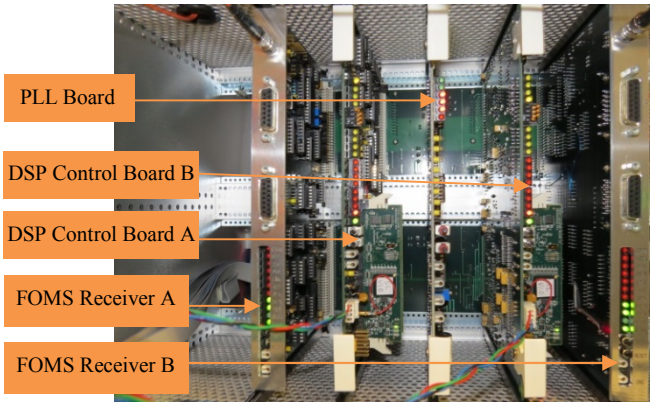

Fig. 6. Five circuit boards inside the firing generator

The signal flow chart and the FG function block diagram are shown Fig. 7.

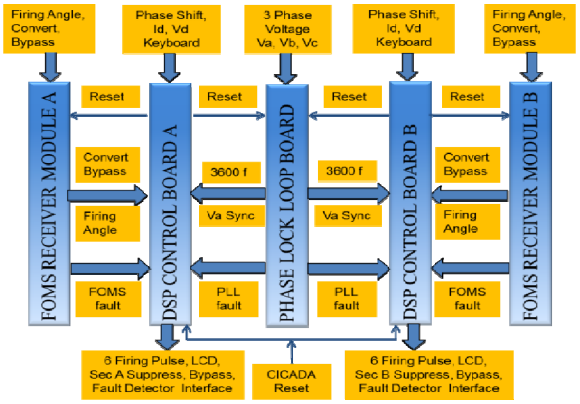

Fig. 7. Firing generator function block diagram

C. *Phase Lock Loop Board*

A phase lock loop (PLL) circuit is used for the phase synchronization of the input variable frequency AC voltage. One advantage of the PLL is that its operation is free from waveform distortions and transients. A PLL consists of a phase detector, a regulator (or low-pass filter) and a voltage controlled oscillator (VCO). The reason to use 12 phase generator is that the ripple frequency will increase with the number of phases, allowing a higher bandwidth for the PLL [3]. An analog multiplexer is used as a phase detector (PD). The output voltage from the PD is filtered by the loop filter which controls the VCO (VFC320) to output a digital pulse train with repetition rate at 3600*f. The PLL board also sends a synchronization pulse which has the same phase information as the input voltage V_a to the DSP control board. The PLL circuit board function block diagram is shown in Fig. 8.

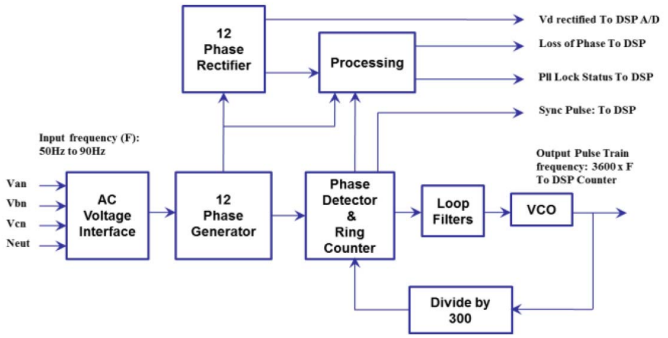

Fig. 8. PLL circuit board function block diagram

D. *DSP Control Board*

DSP control board is the key component in the FG. TI TMS320F28335 DSP is selected for the new FG design. The DSP Enhanced Capture (ECAP) module is used to accept the PLL pulse as the counter clock at 3600*f Hz. Each pulse is 0.1 degree. The firing angle can be calculated based on the pulse count. The minimum time between the two clock pulses for 90 Hz AC input is about 1/3600/90=3.086 µsec. One DSP can't handle all the tasks during this short interval. The typical time for the DSP for the firing angle limit calculation is about 20 µsec. To solve this problem, two DSP are used. One is called the master DSP and the other is called the slave DSP. The signal flow chart for the master and the slave DSP is shown in Fig. 9.

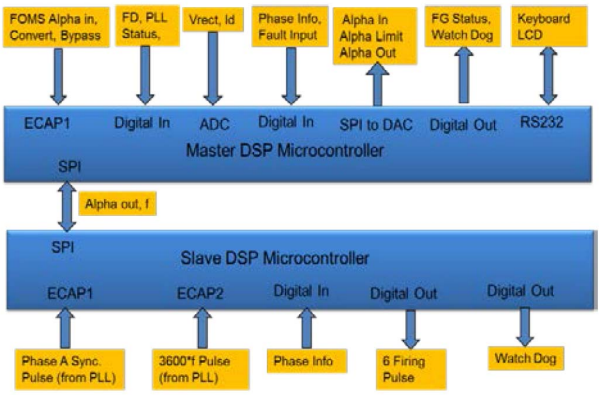

Fig. 9. Firing generator master and slave DSP inputs and outputs

The master DSP has the following function:

- Receive the input firing angle α from the FOMS receiver board and calculate the AC voltage frequency *f* from the PLL board input pulse.
- AC input voltage and load current measurement using the internal 12 bit analog to digital converter.
- Real time firing angle α limit calculation based on the equation:

$$\alpha_{\max} = \cos^{-1}\left[-\cos\gamma + \frac{4\pi f L_c I_d}{\sqrt{2}V}\right] \quad (1)$$

where:

γ = Margin angle (adjustable from 15º to 45º)

L_c = Commutating inductance

f = AC source frequency

I_d = DC load current

V =Rectifier transformer line-to-line AC rms voltage

- Sending the final α to the Slave DSP using the Serial Peripheral Interface (SPI) protocol.
- Update the front panel LCD display information.

The master DSP software flow chart is shown in Fig. 10.

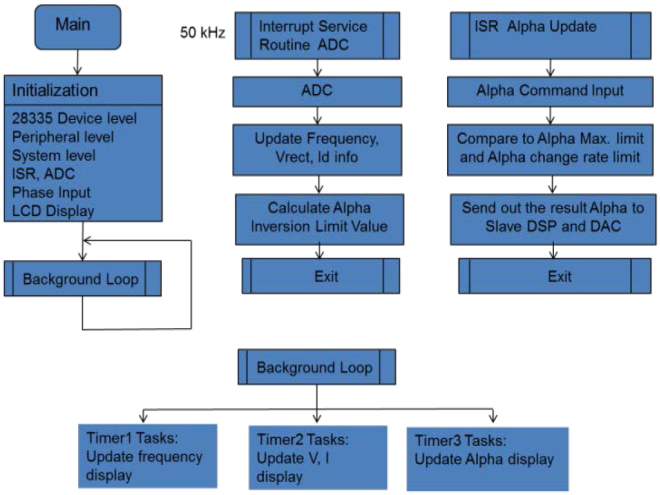

Fig. 10. Firing generator master DSP software flow chart

The slave DSP is dedicated to generate 6 thyristor firing pulses. The time to run each interrupt service routine (ISR) is less than 2 µsec. It has the following function:

- Receives 3600*f pulse train as the pulse counter input from the PLL board.
- Reset the pulse counter when the phase A synchronization pulse is received.
- Update the new firing angle α from the master DSP.
- Generates 6 thyristor pulses.

The slave DSP software flow chart is shown in Fig. 11.

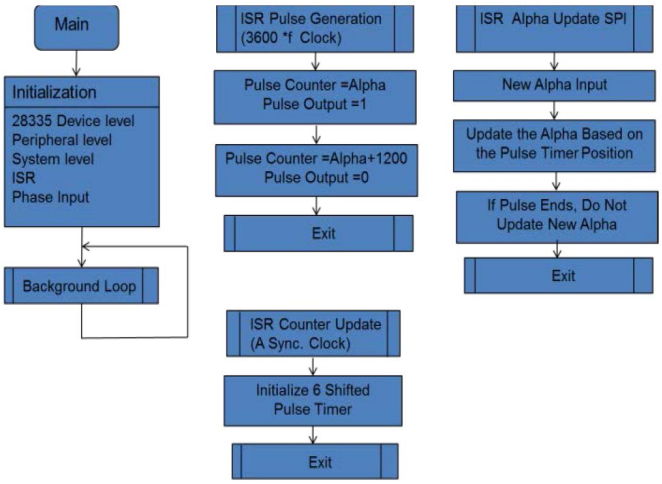

Fig. 11. Firing generator slave DSP software flow chart

A Xilinx CPLD is used on the DSP control board to handle all the fault signals either from the internal circuit boards or from the fault detector. Under any fault conditions, the CPLD blocks all the firing pulses to zero and sent the bypass command to the bypass module.

III. Test Results

Extensive testing was performed to ensure the function of the new FG. Typical results are shown in this paper. During the plasma shot, the input voltage may experience a sudden phase angle change. One of the important tests is the phase angle jump test for the PLL circuit. The Fig. 12 shows the test result with 90º phase jump. The input three phase AC voltage frequency is 75 Hz. The PLL circuit can recover in less than 50 msec.

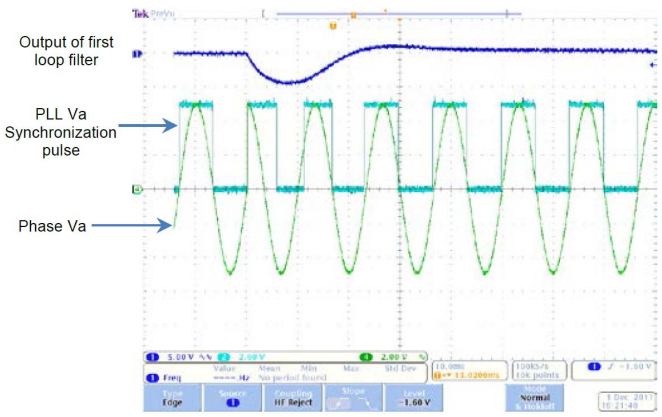

Fig. 12. PLL response to a 90 degree phase step input, 75Hz 3 phase.

There is always some transient noise in the input AC voltage source. To simulate this situation, a noise pulse is injected to phase V_a with the same amplitude. The test result in Fig. 13 shows that VCO control voltage is very steady. The PLL circuit is immune to the transient noise.

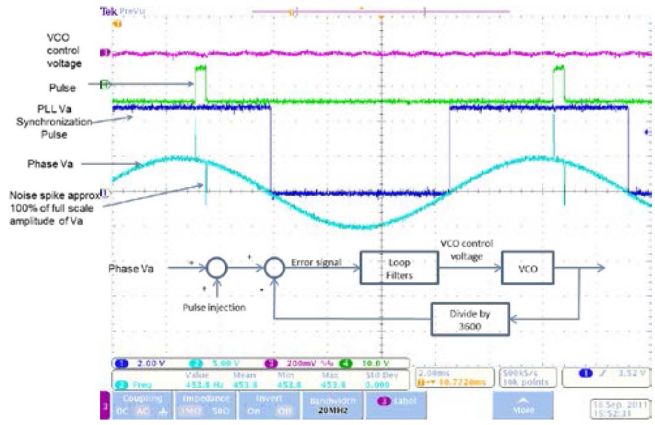

Fig. 13. The PLL transient noise test

The old analog FG designed by Transrex was in service for more than 30 years. The dummy load test is used to compare the performance between the old FG and the new FG. A stair case current is required from the real time computer. The test result using the old FG (black one, 144817) and the new FG (red one, 144803) is shown in Fig. 14. This result shows that in rectifier mode, the old FG and the new FG are equivalent. In inverter mode, the new inversion angle limiter in the new FG works better than the old FG.

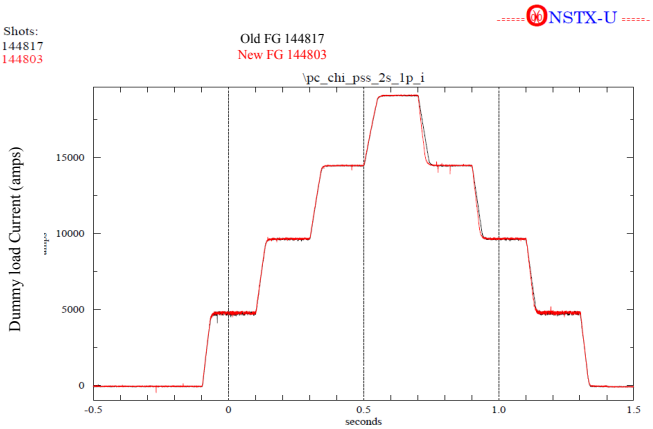

Fig. 14. The comparison test using the old FG and the new FG

The new FG has been used in the NSTX upgrade power supplies. Fig. 15 shows the test shot for the Ohmic Heating (OH) coil power supply under 68 Hz input AC voltage.

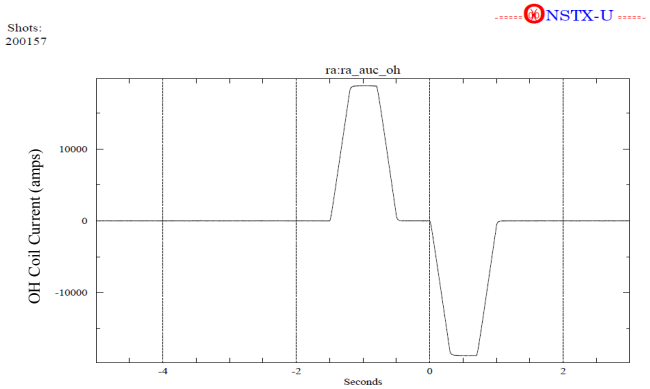

Fig. 15. Test shot for the OH coil power supply

IV. CONCLUSIONS

A new FG has been designed and implemented using a TI DSP. It has been in development and test now for three years. Several hundred NSTX-U test shots have been performed using the new FG without plasma. The tests results have demonstrated excellent reliability and performance. However the full demonstration of operation under conditions with plasma awaits successful results that are anticipated during the upcoming NSTX-U 1st plasma campaign.

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