Princeton Plasma Physics Laboratory

PPPL-4103

PPPL-4103

Development of a Universal Networked Timer at NSTX

P. Sichta, J. Dong, J.E. Lawson,
G. Oliaro, and J. Wertenbaker

September 2005

PPPL
PRINCETON PLASMA
PHYSICS LABORATORY

Prepared for the U.S. Department of Energy under Contract DE-AC02-76CH03073.

PPPL Report Disclaimers

Full Legal Disclaimer

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, nor any of their contractors, subcontractors or their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or any third party's use or the results of such use of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof or its contractors or subcontractors. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

Trademark Disclaimer

Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof or its contractors or subcontractors.

PPPL Report Availability

This report is posted on the U.S. Department of Energy's Princeton Plasma Physics Laboratory Publications and Reports web site in Fiscal Year 2005. The home page for PPPL Reports and Publications is: http://www.pppl.gov/pub_report/

Office of Scientific and Technical Information (OSTI):

Available electronically at: http://www.osti.gov/bridge.

Available for a processing fee to U.S. Department of Energy and its contractors, in paper from:

U.S. Department of Energy
Office of Scientific and Technical Information
P.O. Box 62
Oak Ridge, TN 37831-0062

Telephone: (865) 576-8401

Fax: (865) 576-5728

E-mail: reports@adonis.osti.gov

National Technical Information Service (NTIS):

This report is available for sale to the general public from:

U.S. Department of Commerce
National Technical Information Service
5285 Port Royal Road
Springfield, VA 22161

Telephone: (800) 553-6847

Fax: (703) 605-6900

Email: orders@ntis.fedworld.gov

Online ordering: http://www.ntis.gov/ordering.htm

Development of a Universal Networked Timer at NSTX

P. Sichta, J. Dong, J.E. Lawson, G. Oliaro, J. Wertenbaker
Princeton Plasma Physics Laboratory, Princeton, USA

Abstract - **A new Timing and Synchronization System component, the Universal Networked Timer (UNT), is under development at the National Spherical Torus Experiment (NSTX). The UNT is a second generation multifunction timing device that emulates the timing functionality and electrical interfaces originally provided by various CAMAC modules. Using Field Programmable Gate Array (FPGA) technology, each of the UNT's eight channels can be dynamically programmed to emulate a specific CAMAC module type. The timer is compatible with the existing NSTX timing and synchronization system but will also support a (future) clock system with extended performance. To assist system designers and collaborators, software will be written to integrate the UNT with EPICS, MDSplus, and LabVIEW. This paper will describe the timing capabilities, hardware design, programming/software support, and the current status of the Universal Networked Timer at NSTX.**

Keywords-data acquisition; network; timing

I. INTRODUCTION

An essential facility for NSTX research is the central timing and synchronization system [1], which is used to synchronize control and data acquisition systems throughout the NSTX experimental complex. Most of the timing system is constructed using 25 year old CAMAC technology which presents maintenance and performance problems. Over the past few years NSTX has been developing a new core timing component based upon an FPGA. The first generation device was called the Multifunction Timing System (MTS) [2], which has been successfully deployed on several NSTX subsystems. This report will describe the salient features of the UNT, including a description of the hardware and software, the current status, and future plans.

II. REVIEW OF THE MTS

The MTS was designed to emulate a variety of practical timing functions and electrical interfaces that in the past were provided by several types of CAMAC modules. The device had six channels, each of which could be dynamically programmed to perform the desired timing function. There were a variety of ways the user could program the timing channels: a Windows DLL, a VisualC++ GUI, LabVIEW, and MDSPlus or EPICS (via LabVIEW). The MTS PCI-board was typically installed in a rack-mount PC along with other data acquisition boards, forming a PC-based control and data acquisition system.

Work performed under the auspices of the US Department of Energy by Princeton Plasma Physics Laboratory under Contract No. DE-AC02-76-CH0-3073.

A. *Timing Functions*

Reference [2] contains a more thorough description of the timing functions and performance capabilities of the MTS. These are the main features of the UNT:

- Eight channel device.
- Timing functions include event-decoding, delay, triggers, gates, clocks, pulse counting.
- Timing functions triggered by software or external signals.
- 100 nS timing resolution.
- 256 event codes on link.
- Supports 1 MHz and 10 MHz link/carrier.

B. *Enhanced Clock Capabilities*

The MTS is compatible with the existing NSTX clock system, but it will also support an enhanced (future) clock system. The additional capabilities include:

- A base (carrier) frequency upgrade from 1 MHz to 10 MHz.
- 100 nanosecond timing resolution, rather than (up to) 1 millisecond.
- Fiber optic Facility Clock ports.
- Additional event decoding, from 16 events to 256.

III. UNT SYSTEM DESIGN

One of the shortcomings of the MTS was its packaging. It required a computer with a PCI bus slot and a cable to attach to the external isolation-circuit board. Although the PCI bus is currently the most popular it is already diminishing in lieu of PCI busses with extended performance. The MTS' PCI-bus requirement was a hindrance in interfacing non-PCI control system technologies such as PLC, VME, CompactPCI, PC-104, and PCI-X. This presents a problem for NSTX researchers and collaborators who often bring modern and unique systems for integration onto NSTX.

A primary design criterion for the next generation timing device was to maximize the product's versatility and longevity. Experience has shown that over the lifetime of a fusion device, hardware and software technologies evolve through several generations. Things that were popular and easily supported at

the beginning of the research project become costly and difficult to maintain in the project's latter years. Industry standards and open software will be used to minimize these life-cycle issues.

The UNT is based upon two of the most enduring international standards. Physically, the device is compliant with the IEC 60297 standard (19" rack-mount equipment). Communications for programming and configuring the timing channels employ the IEEE 802 standards (Ethernet). In addition, the world's leading industrial Ethernet protocol [3] Modbus TCP/IP will be used. Most computers, operating systems, and programming and scripting languages can access the network. These aforementioned attributes will lengthen the useful lifetime of the UNT.

A. *Improvements upon MTS*

- The system has been repackaged:
  - no longer dependent on PCI bus technology.
  - eliminated the external interface board and cable.
- The device is programmable via the network.
- Number of channels increased to 8.
- Supports fiber optic as well as 'copper' link interfaces.
- Uses a larger Xilinx FPGA (300,000 gate version).
- Upon power-up, the FPGA is auto-loaded from Flash.
- Upgraded the interface circuitry.

B. *Network Issues*

Using a tcp/ip network in a control system is often a concern due to the tcp/ip protocol's unpredictable latency. In the UNT application, network latency does not present a problem. The use of the network is only for configuration and status, no real-time functions are required. For example, the network is used to configure a channel to decode a link event, delay a specified time, and then output a trigger pulse. This configuration is usually done well before the actual link event is expected to come.

Another network consideration is cyber-security and channel configuration control. The UNT is fully programmable and configurable over the network. Unauthorized access to the device by a malicious user might cause the control/data-acquisition system to malfunction. The current network-interface device used on the UNT does not have a built-in firewall. The laboratory's cyber-security infrastructure, and in particular, configuration of the network port can restrict access to only authorized users or computers. Lantronix Inc. has recently released a network interface device called the Xport-AR. This includes network security features and will be considered for the next fabrication cycle.

IV. HARDWARE DESIGN

Fig. 1 shows a block diagram for the UNT. The physical assembly is modular so that portions of the system can be upgraded when the on-board 'silicon' becomes obsolete. It consists of the chassis, a 5 volt power supply, and three circuit boards: the Facility Clock Link Interface, the Main Board, and the Auxiliary Board. The 4-layer printed circuit boards were designed in-house using a free software package, ExpressPCB.

The Facility Clock Link Interface comes in two models, one for twinaxial cable and the other for fiber optic connections. The link interface was separated from the main board so that different fiber optic components could be used, anticipating a change in fiber optic technology. Both types of interfaces provide electrical isolation to eliminate ground loops.

The Main Board contains the following: Lantronix Xport-Xe network interface module, Texas Instruments MSP430 microcontroller (MCU), Xilinx Spartan-IIE XC2S300E FPGA, Flash PEROM (programmable and erasable read only memory), and (16) opto-isolated timing signal inputs. There are also several jumpers on the board that are used to inform the FPGA program about the configuration of the system, for example, which type of auxiliary board is attached.

The Type 1 Auxiliary Board contains (24) timing signal outputs, three for each of the eight channels. One output is (pulse) transformer-coupled, one is an opto-coupler, and the third is a non-isolated line driver.

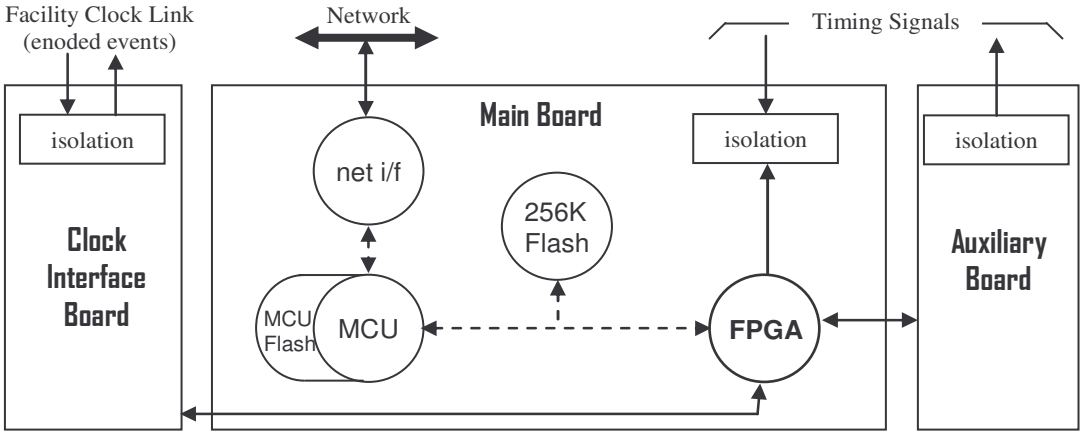

Figure 1. Block Diagram of the Universal Networked Timer.

A. *Device Morphing*

Due to the modular and reprogrammable nature of the UNT, it can be programmed and reconfigured to support a variety of control and data acquisition functions that are vastly different from the initial timing application. The first application of this is the Clock Encoder. One of the UNT's primary functions is to decode encoded events off of the Facility Clock Link. The Clock Encoder does the opposite; it encodes events onto the link.

The FPGA has been programmed to implement the timing functions of the CAMAC model 401 Clock Encoder. Another type of auxiliary board will be used, a Type 2 Auxiliary Board. Instead of (24) outputs this board will have (16) opto-isolated timing signal inputs, for a total of (32) inputs. The FPGA pins that connect to the Auxiliary Board will be reconfigured from outputs to inputs. Each input trigger pulse will immediately generate a (programmable) clock event onto the Facility Clock link. The UNT will be able to simultaneously generate events onto two separate Facility Clock links, each having a different carrier frequency. This would be useful at NSTX where a 1 MHz carrier is needed for legacy CAMAC clock decoders (model 404), but UNT and MTS devices could use the enhanced timing capability offered by a 10 MHz carrier.

Additional programs for the FPGA could implement other functions, such as a strobed digital input module, a multi-channel counter, or a digital input/output device. In summary, the same basic, physical device and development processes can be used to make the UNT suitable for a wide variety of control system applications. The Auxiliary Board and the front panel will be tailored to each specific application.

V. SOFTWARE DESIGN

A wide range of software skills were required to develop UNT. The software functions, development tools, and user programming interfaces will be described in this section.

A. *Device Software*

There are two 'processors' in the UNT device, the MCU and the FPGA. In addition to power-up sequencing the MCU is used to interface three on-board components: the network interface, flash memory, and the FPGA as shown in Fig. 2.

The MCU interprets the network's incoming Modbus TCP/IP messages and if valid, performs the requested action. Typical actions are to send timing channel values to the FPGA, for example, to program a delay between a clock link event and an output trigger for a transient digitizer. The interface also supports up/down-loading FPGA code to the PEROM. Development tools used for the MCU code include:

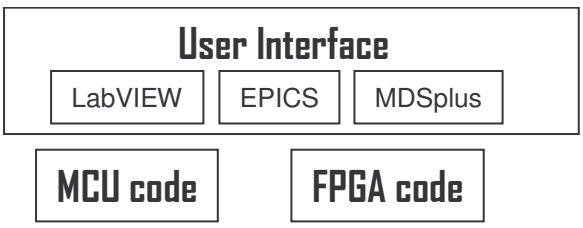

Figure 2. Software for the Universal Networked Timer.

- Microsoft Inc. Visual C++ (editor & download mgr)
- mspgcc - The GCC toolchain for the Texas Instruments MSP430 MCUs (free, open) [4]

As described in [2] the FPGA code is produced by first using a schematic-entry tool. The schematic is drawn, and then converted to VHDL, and then compiled into a file of S-records. This binary image is transferred over the network (or via JTAG) into the flash PEROM. The FPGA runs its 'code' in hardware (firmware) so real-time performance is achieved. The timing accuracy and synchronism of the UNT is a function of the FPGA, and has been measured to be about ten nanoseconds. Development tools used for the FPGA code include:

- Xilinx Inc. ISE WebPack (free)

B. *User-Programming*

The development team will provide documentation and programming interfaces for 'the user' of the timing device. Programming the various timing functions in the UNT is done over a tcp/ip network using an open, de facto standard communications protocol, Modbus TCP/IP [5]. A series of Modbus Application Protocols (MBAP) have been specified for communicating with the UNT [6].

Software support will be developed for NSTX's major application software environments: National Instruments Inc. LabVIEW, Research Systems Inc. IDL, and the open, collaborative software packages EPICS [7] and MDSplus [8].

VI. STATUS

The UNT is currently under development and will see its first deployment during the upcoming (2006) NSTX run period. The chassis and all three circuit boards have been fabricated. The MCU code is nearing completion. LabVIEW support has been written for the UNT. This consists of about (25) Virtual Instruments (VI) as well as a stand-alone application. The EPICS, MDSplus and IDL user interfaces have not been designed yet.

The initial UNT installation will use LabVIEW, since LabVIEW can communicate with the UNT, as well as with EPICS and MDSplus. The Clock Encoder FPGA coding is complete and has been tested using the MTS as a development platform. The encoder can be deployed using the existing UNT hardware in a single-link, 16-event configuration. To use dual-link outputs and have a 32-event system, a Type 2 auxiliary board and a slightly modified link interface board are needed.

Two important system design considerations that need to be carefully considered by the user are cyber-security and configuration control. The UNT is fully programmable and configurable over the network. Unauthorized access to the device by a malicious user might cause the control/data-acquisition system to malfunction. The current network-interface device used on the UNT does not have a built-in firewall. The laboratory's cyber-security infrastructure and

configuration of the network port can be used to restrict access to the UNT to only authorized users or computers. Adding authentication software to the MCU code and MBAP specifications is another solution being considered.

One of the MBAP will be used to interrogate the UNT to determine software revision (MCU and FPGA) and hardware configuration. The application programmer should use this information to verify that they are communicating with the correct type of device.

VII. CONCLUSION

Building upon the successful FPGA-based Multifunction Timing Device, the Universal Networked Timer is nearing completion and first deployment at NSTX. The product's design basis includes application-flexibility, hardware and software modularity, and a foundation built upon enduring industry standards. The UNT is compatible with the existing NSTX clock system, but will also support an enhanced clock system in the future. The UNT is a networked device, so it will be able to be used with all control and data acquisition systems regardless of the hardware technology.

A wide range of expertise has been required for this project. This includes learning integrated development environments for the FPGA code and the MCU code; programming in C, LabVIEW, and IDL; EPICS and MDSplus device-level (network) programming; network and cyber-security administration; understanding Modbus protocols, interface circuit design; printed circuit board layout, fabrication, test, and developing technical documentation. Throughout the design process, documentation and interface specifications were essential since the design team personnel worked on 'their' part sporadically.

One of the guiding principals in the development of the UNT was that it be impervious to technological-obsolescence. With the standards used in the design, together with the hardware and software modularity, and relying on the most common computing element, the network, the outlook for achieving this goal looks promising.

ACKNOWLEDGMENT

The development of the Universal Networked Timer would not have been possible without the vision, encouragement, and leadership of my colleague and mentor, Gary Oliaro. This innovative device is just one of the many contributions to fusion research that Gary has fostered over the past 32 years.

REFERENCES

[1] J. Montague 'Synchronization of Timing Systems on TFTR,' 14th Symposium on Fusion Engineering, San Diego, CA (1991).

[2] P. Sichta et al, 'Developments to Supplant CAMAC with Industry Standard Technology at NSTX,' Fusion Engineering and Design, vol. 71, Issues 1-4, June 2004, pp 129-133.

[3] ARC Advisory Group, "Industrial Ethernet Worldwide Outlook", September 2005, http://www.arcweb.com/research/pdfs/Study_ethernet.pdf .

[4] Source Forge.Net , "Home Page for MSPGCC", September 2005, http://mspgcc.sourceforge.net .

[5] Modbus-IDA , "Industrial Modbus-IDA Home Page", September 2005, http://modbus.org .

[6] P. Sichta, (unpublished project documents and files), September 2005.

[7] EPICS Home Page , "EPICS Collaboration Home Page", September 2005, http://www.aps.anl.gov/epics .

[8] MDSplus Home Page, "MDSplus Home Page", September 2005, http://www.mdsplus.org .

External Distribution

Plasma Research Laboratory, Australian National University, Australia
Professor I.R. Jones, Flinders University, Australia
Professor João Canalle, Instituto de Fisica DEQ/IF - UERJ, Brazil
Mr. Gerson O. Ludwig, Instituto Nacional de Pesquisas, Brazil
Dr. P.H. Sakanaka, Instituto Fisica, Brazil
The Librarian, Culham Science Center, England
Mrs. S.A. Hutchinson, JET Library, England
Professor M.N. Bussac, Ecole Polytechnique, France
Librarian, Max-Planck-Institut für Plasmaphysik, Germany
Jolan Moldvai, Reports Library, Hungarian Academy of Sciences, Central Research Institute for Physics, Hungary
Dr. P. Kaw, Institute for Plasma Research, India
Ms. P.J. Pathak, Librarian, Institute for Plasma Research, India
Dr. Pandji Triadyaksa, Fakultas MIPA Universitas Diponegoro, Indonesia
Professor Sami Cuperman, Plasma Physics Group, Tel Aviv University, Israel
Ms. Clelia De Palo, Associazione EURATOM-ENEA, Italy
Dr. G. Grosso, Instituto di Fisica del Plasma, Italy
Librarian, Naka Fusion Research Establishment, JAERI, Japan
Library, Laboratory for Complex Energy Processes, Institute for Advanced Study, Kyoto University, Japan
Research Information Center, National Institute for Fusion Science, Japan
Professor Toshitaka Idehara, Director, Research Center for Development of Far-Infrared Region, Fukui University, Japan
Dr. O. Mitarai, Kyushu Tokai University, Japan
Mr. Adefila Olumide, Ilorin, Kwara State, Nigeria
Dr. Jiangang Li, Institute of Plasma Physics, Chinese Academy of Sciences, People's Republic of China
Professor Yuping Huo, School of Physical Science and Technology, People's Republic of China
Library, Academia Sinica, Institute of Plasma Physics, People's Republic of China
Librarian, Institute of Physics, Chinese Academy of Sciences, People's Republic of China
Dr. S. Mirnov, TRINITI, Troitsk, Russian Federation, Russia
Dr. V.S. Strelkov, Kurchatov Institute, Russian Federation, Russia
Kazi Firoz, UPJS, Kosice, Slovakia
Professor Peter Lukac, Katedra Fyziky Plazmy MFF UK, Mlynska dolina F-2, Komenskeho Univerzita, SK-842 15 Bratislava, Slovakia
Dr. G.S. Lee, Korea Basic Science Institute, South Korea
Dr. Rasulkhozha S. Sharafiddinov, Theoretical Physics Division, Insitute of Nuclear Physics, Uzbekistan
Institute for Plasma Research, University of Maryland, USA
Librarian, Fusion Energy Division, Oak Ridge National Laboratory, USA
Librarian, Institute of Fusion Studies, University of Texas, USA
Librarian, Magnetic Fusion Program, Lawrence Livermore National Laboratory, USA
Library, General Atomics, USA
Plasma Physics Group, Fusion Energy Research Program, University of California at San Diego, USA
Plasma Physics Library, Columbia University, USA
Alkesh Punjabi, Center for Fusion Research and Training, Hampton University, USA
Dr. W.M. Stacey, Fusion Research Center, Georgia Institute of Technology, USA
Director, Research Division, OFES, Washington, D.C. 20585-1290

The Princeton Plasma Physics Laboratory is operated
by Princeton University under contract
with the U.S. Department of Energy.

Information Services
Princeton Plasma Physics Laboratory
P.O. Box 451
Princeton, NJ 08543

Phone: 609-243-2750
Fax: 609-243-2751
e-mail: pppl_info@pppl.gov
Internet Address: http://www.pppl.gov