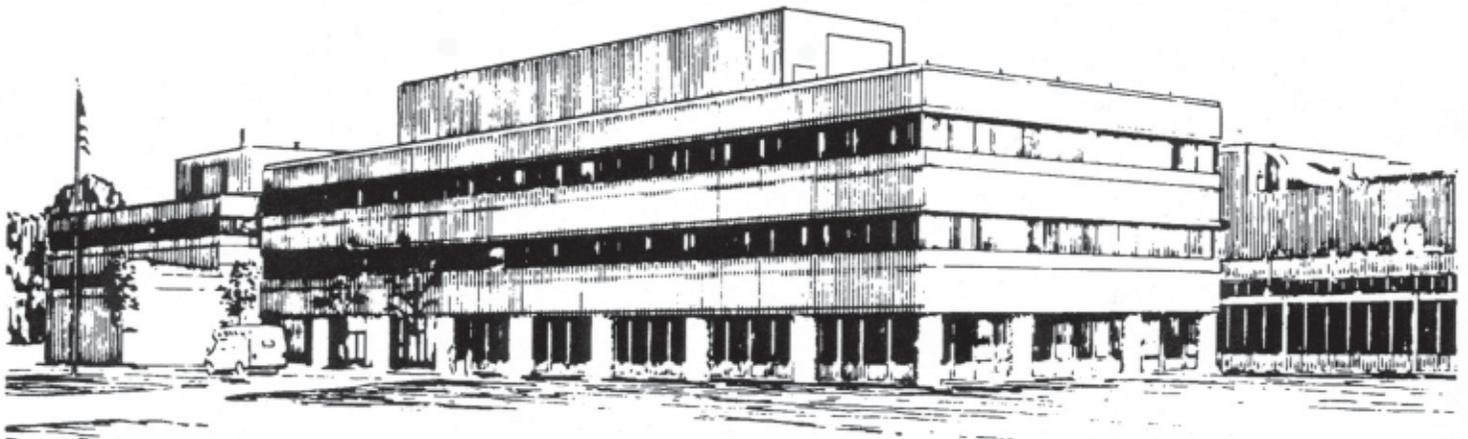# National Spherical Torus Experiment Real Time Plasma Control Data Acquisition Hardware

by

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Availability

NATIONAL SPHERICAL TORUS EXPERIMENT REAL TIME PLASMA CONTROL DATA ACQUISITION HARDWARE

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ABSTRACT

The National Spherical Torus Experiment (NSTX) is currently providing researchers data on low aspect-ratio toroidal plasmas. NSTX's Plasma Control System adjusts the firing angles of thyristor rectifier power supplies, in real time, to control plasma position, shape and density. [1] A Data Acquisition system comprised of off-the-shelf and custom hardware provides the magnetic diagnostics data required in calculating firing angles. This VERSAmodule Eurocard (VME) bus based system utilizes Front Panel Data Port (FPDP) for high-speed data transfer. Data coming from physically different locations is referenced to several different ground potentials necessitating the need for a custom FPDP multiplexer. This paper discusses the data acquisition system configuration, the in-house designed 4 to 1 FPDP Input Multiplexing Module (FIMM) and future expansion plans.

1. INTRODUCTION

NSTX

The National Spherical Torus Experiment (NSTX) at the Princeton Plasma Physics Laboratory (PPPL) is designed for studying the physics of the Spherical Torus, a low aspect ratio variant of the standard tokamak that can maintain plasma pressure with a lower magnetic field. [2] Reducing magnetic fields could lead to a smaller and thus less expensive fusion reactor. [3,4]

PLASMA CONTROL

The Plasma Control System is the most advanced of all the control systems (approximately 50 in total) in use on NSTX. [5,6] At a sampling rate of 5 kHz, data from up to 160 magnetic diagnostics, including plasma current, magnetic coil currents, magnetic flux and local magnetic fields are utilized by the Plasma Control Software (PCS). The PCS, developed by General Atomics, provides closed loop control of magnetic coil currents, plasma current, outer gap and vertical position. [7] Plasma shape, elongation and trianglularity, is currently under open loop control. However, Real Time Equilibrium Reconstructed Fitting Code (rtEFIT), also developed by General Atomics, is currently being integrated into the PCS to provide closed loop control of plasma shape at a 1ms rate.

COAXIAL HELICITY INJECTION

NSTX's investigation of non-inductive plasma start-up utilizes Coaxial Helicity Injection (CHI). CHI is a method of heating the plasma by injecting a current through it. The inner and outer vacuum vessel walls, which are insulated from each other by ceramic breaks, are used as electrodes. A 1kV potential drives up to 50kA, which in the presence of the toroidal fields, results in plasma current on the order of ten times as large (500kA). [8] Because of this potential difference, magnetic diagnostics referenced to the inner and outer vacuum vessel walls must be electrically isolated from each other and from ground.

GROUNDS

The inner and outer vacuum vessel referenced diagnostics are also isolated from the magnetic coil current diagnostics creating Plasma Control System data at three different ground potentials. These vessel and coil diagnostics are also physically located from each other by approximately 175 meters.

2. SYSTEM CONFIGURATION

The Real Time Plasma Control Data Acquisition System is based on industry standard busses and acquisition, control and interface hardware. (See Figure 1) System requirements also necessitated the need for in-house designed hardware as well.
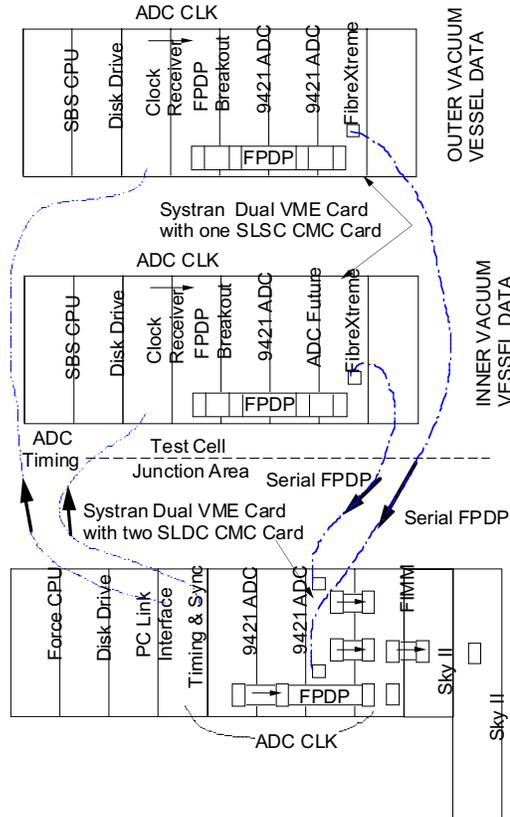

Figure 1. NSTX's Real Time Plasma Control Data Acquisition System Block Diagram

COMMAND & CONTROL BUS
The VERSAmodule Eurocard (VME) bus is an open computer architecture based on the VERSAbus electrical specification and Eurocard mechanical format. Three different height VME boards can be plugged onto a backplane with up to 21 slots. Two 6U high crates are located in the Test Cell. One each for data referenced to the Inner Vacuum Vessel and Outer Vacuum Vessel walls. The third, a combination 6U and 9U high crate is located 175 meters away in a room near the magnetic coil power supplies called The Junction Area.

PROCESSORS
The two Test Cell crates contain SBS V5B VME computers running Windows 2000 as slot 1 crate controllers. These computers are used to configure the data acquisition boards over the VME bus. The processors are not needed after configuration and the operating system is shut down.

The Junction Area Crate uses a Force CPU-50G as the slot 1 crate controller. All outside communication via Ethernet is routed through this processor. A 6U SKY II is used as the master real time processor, while the 9U SKY II is used as the slave. Communication between the two Sky computers is via the VME P2 connector mounted Sky Channel back plane bus.

DATA TRANSFER BUS
Because of the delay time in asking for and granting the VME bus to different modules, the VME bus is not very well suited for small data transfers that occur often. Thus for data transfer between the digitizers and the real time computer, the Front Panel Data Port (FPDP) bus is utilized. The FPDP bus is a 32-bit parallel synchronous bus providing data transfer between two or more VME boards, in one direction, at rates up to 160MB/s with a 40MHz clock. [9] Front panel connections at up to 5 meters are via 80 conductor ribbon cables. Multiple FPDP busses can co-exist in a VME crate and data from multiple boards may be combined into a composite data stream carried via one ribbon cable, but only one board can act as a Transmitter Master (TM). The TM provides the FPDP clock as well as other timing signals for the bus.

SERIAL DATA INTERFACE
Fiber optic interfacing is a natural solution for the three electrically isolated and physically separated crates. Systran's FibreXtreme Simplex Link extends FPDP connections to 10km over fiber cable while preserving FPDP's high data rates and low latency via a dedicated data link from a single transmitting card to one or more receiving cards. The FibreXtreme receiving cards act as TMs.

DATA AQCUISITION

At the center of the Plasma Control System is Merlin's 9421 Analog Input Module. The module interfaces to the VME bus and the FPDP. With 12 bit resolution, up to 32 differential input channels can be sampled simultaneously triggered by an Analog to Digital Convert (ADC) command via the FPDP bus. Data is "packaged" so that each 32 bit FPDP word contains two 12 bit channels. Each channel has four extra bits (32/2 = 16, 16 - 12 = 4) that are hardwired as logic 0's. During NSTX shots the sample rate is 5kHz. Between shots, data is sampled at a 1Hz rate. Up to seven modules can be used in one VME crate. This is accomplished by configuring the left most module as FPDP Transmitter Master (TM) via software commands from the SBS or Force Computer over the VMEbus.

ADC CLOCK INTERFACE

Two in house designed and fabricated modules generate and distribute the ADC Clock to the ADCs. The Timing & Synchronization Module, in the Junction Area crate, generates the clock signal whose rate depends on signals from the NSTX timing system and transmits the ADC Clock to the local FIMM via copper and to the two Test Cell crates over fiber optic cable. Clock Receiver Modules in each Test Cell Crate receive the optical signal, convert the optical signal to an electrical signal and transmit the ADC Clock to a FPDP Break Out Module, which then places it on the POI 1 line of the FPDP bus for use by the ADCs.

3. FIMM

The FIMM is a double width module that uses the VMEbus for power and ground only. (See Figure 2) Its two-board design along with surface mounted components enables the module to fit into a 6U high card. Up to four independent FPDP inputs are terminated by the FIMM acting as Receiver Masters and time multiplexed into one FPDP Transmitter Master output. A status light for each input and output indicates nominal shot or between shot activity as well as error conditions.

The Junction Area's FPDP bus must be plugged into the FIMM Input Port #1. Only Port #1 is configured to carry the ADC

Clock. This eliminates the need for an FPDP Break Out module in the Junction Area crate since the ADC Clock is fed directly from the Timing & Synchronization Module to the FIMM. The Timing & Synchronization Module feeds the ADC Clock to FPDP Break Out Modules in other crates via fiber optic links and the Clock Receiver Module. The FPDP Break Out Modules receive the ADC Clock and then place it on the FPDP bus PIO 1 lines.

The FIMM and Plasma Control System are configured to transfer FPDP data without the handshaking or flow control of the SUSPEND* signal. Generated by an FPDP Receiver or Receiver Master (RM), the SUSPEND* signal informs the data transmitter of a pending buffer overflow. Testing has indicated that data transfer with an ADC Clock of almost 10KHz is possible without the SUSPEND* signal.
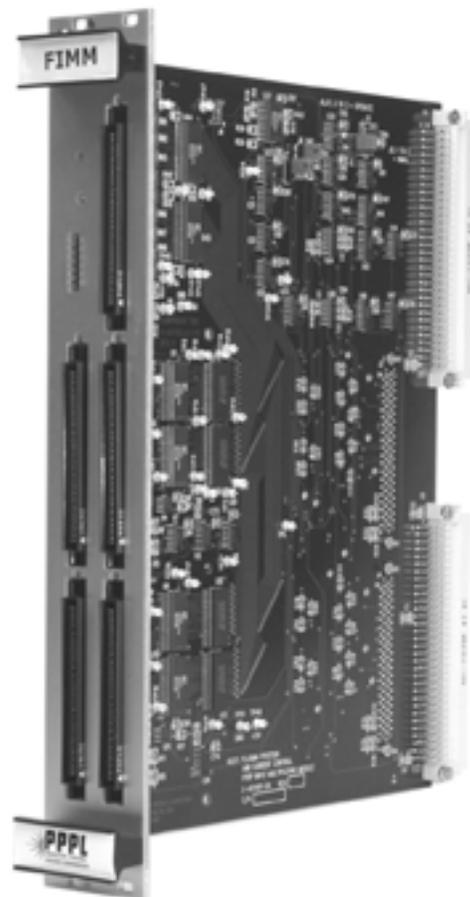

Figure 2. 1 FPDP Input Multiplexing Module (FIMM) designed by R. J. Marsala

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Any FIMM Input Port without a Transmitter Master (TM) connected is considered inactive and ignored. Higher numbered Input Ports above the first inactive port will also be ignored even if a TM is connected.

For Plasma Control System use, the FIMM is configured for Unframed Data format that has no synchronization of the data. This can be changed if needed, by way of jumpers, to the Single Frame Data format, which is intended for data to be synchronized between blocks.

Data can be clocked in at the FPDP maximum rate of 40MHz while jumpers select the output rate of either 8MHz or 16MHz. FIMM output transmission starts with the lowest number ports first after every active FPDP input port has loaded into the FIFOs. After the last active input channel has emptied all stored data, transmission stops. (See Figure 3) The FIFOs are 32 bits by 256 words, large enough to store data from sixteen 32 channel Analog Input Modules.
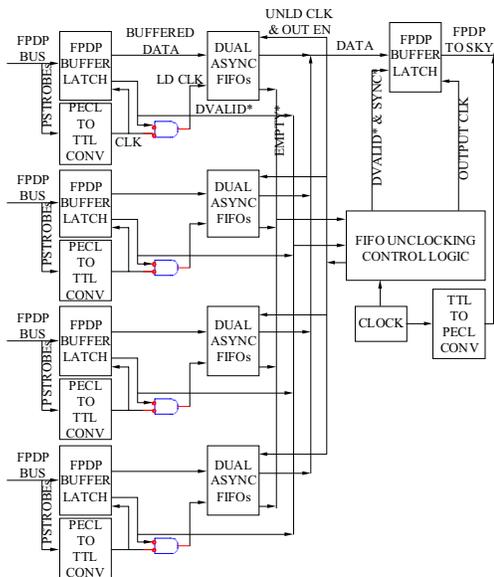

Figure 3. FIMM Functional Block Diagram

The FIMM is compliant in electrically terminating all FPDP signals. Some FPDP signals, however, are not used in the Plasma Control System and were therefore not included in the FIMM design.

4. FUTURE EXPANSION

NSTX
Several more Analog Input Modules will be added to the Outer Vacuum Vessel referenced VME crate in the immediate future to process data from new magnetic coils being added to NSTX. In the longer term, input data from the Thompson Scattering diagnostic (which measures electron density and temperature) and the Motional Stark Effect (MSE) polarimetry (which measures the internal magnetic structure of the plasma) will be added to help control the plasma equilibrium.

A scheme currently under investigation would utilize the FPDP in the 9U Sky II as an output port to control other systems. The first system to be controlled by FPDP would be the Neutral Beams system. The power output of the three Neutral Beam sources could be notched, in real time, during shots.

Another prime candidate for FPDP control would be the rectifier firing angles. This would eliminate the need to access the VME bus every millisecond to transmit the data to the PC Link Interface module in the present system.

Lastly, the FPDP output could also be used to control valves on the Gas Injection System and real time phase control of the radio frequency heating antenna.

NATIONAL COMPACT STELLARATOR EXPERIMENT
The National Compact Stellarator Experiment (NCSX) is now in conceptual design. The Real Time Plasma Control Data Acquisition System will be expanded to control NCSX as well as NSTX. Since the power system will be shared between the two machines, the Junction Area Digitizers will remain the same. Additional optically coupled signals from Systran modules in the NCSX test cell will be input to the Junction Area VME crate. Selection of the inputs and control of NSTX or NCSX will be under software control.

5. ACKNOWLEDGEMENTS

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